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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,263	02/09/2004	Akira Ito	1875.2590001	8570

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,263	ITO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,163,180 to Eltoukhy et al. (cited by applicant).

Regarding claim 1, Eltoukhy discloses a method of programming an anti-fuse device, comprising: forming a channel (figure 3, area under 16a) between a source region (26) laterally spaced from a drain region (28a) in a substrate (12); forming a gate oxide (14; figure 3) on the channel; forming a gate (16) on the gate oxide (also see column 4, lines 25-65); forming lightly doped source and drain extension regions (18a and 20a) in the channel that cumulatively occupy more than half of the channel (figure 3); and programming the anti-fuse device through application of power to the gate and one of the source or drain regions to break down the oxide and minimize resistance (column 2, lines 1-8; column 3, lines 37-55; column 5, lines 26-68).

Regarding claim 2, Eltoukhy discloses that the substrate is lightly P doped (column 4, lines 29-33; figures 1-4).

Regarding claims 3 and 4, Eltoukhy discloses doping the source and drain regions as well as the source and drain extension regions with N-type material (column 4, line 62 – column 5, line 15).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eltoukhy et al. in view of U.S. Patent No. 6,515,931 to Marr et al. (cited by applicant)

Regarding claims 5 and 6, Eltoukhy fails to disclose that the source, drain, and extension regions are p-type.

Marr discloses that an anti-fuse device can equivalently be formed using N-type source/drain regions and P-type source/drain regions (figures 1-2; column 3, lines 25-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the anti-fuse device fabrication method of Eltoukhy, such that the source, drain, and extension regions are doped with P-type material, as suggested by Marr. The rationale is as follows: A person having ordinary skill in the art would have been motivated to P-type source, drain, and extension regions, because NMOS and PMOS anti-fuse devices are recognized as analogous and equivalent in the art (see Marr, column 3, lines 25-41), and it is well within the purview of a person having ordinary skill in the art to reverse the polarities of the doped regions of the device (i.e. to select either an NMOS or a PMOS device (also see Marr, figures 1 and 2).

Regarding claim 9, Eltoukhy discloses doping the substrate with a P-type material (figures 1-4), but fails to disclose forming the source and drain regions in an N-well region formed in the substrate.

Marr disclose an anti-fuse in which the source and drain regions (16 and 18) are formed in an N-well layer (12) doped into a P-type substrate (14; figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the anti-fuse of Eltoukhy, such that the device is formed in an N-well, as taught by Marr. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide the device in an N-well, because doing so prevents the formation of parasitic diodes between any regions of the anti-fuse device (Marr, column 4, lines 32-43). Also, placing the device in an N-well allows the anti-fuse to be compatible with any polarity or doping strength of the substrate, which makes it viable for CMOS fabrication, as is appreciated by one skilled in the art.

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eltoukhy et al in view of U.S. Patent No. 6,326,651 to Manabe (cited by applicant).

Eltoukhy fails to disclose a deep N-well region or a deep P-well region formed within the substrate beneath the source, drain, and channel region.

Manabe discloses a deep N-well region (109) and a deep P-well region (111) formed within the substrate (100) beneath the source, drain, and channel regions (figure 4) of their respective MOS transistors in the CMOS device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the anti-fuse structure of Eltoukhy, such that a deep N-well or a deep P-well is formed within the substrate beneath the source, drain, and channel regions, as taught by Manabe. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a deep N-well or P-well, so that it can act as a channel stopper region, to define the size and spread of the MOS channel (see Manabe, column 7, lines 1-11).

Allowable Subject Matter

6. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: In the examiner's opinion, a person having ordinary skill in the art would not have been motivated to provide a MOSFET-like device having source and drain extension (Ldd) regions that join or overlap each other under the gate. Conventionally, for a MOSFET-like antifuse device, the device structure is substantially similar to an operative MOSFET, with the channel region lightly doped with an opposite polarity to the source and drain regions. In the present invention, however, in order to achieve the specific purpose of providing a more uniform fuse resistance for an antifuse-type MOSFET-like device, the source and drain extension regions are joined, essentially lightly doping the channel region with dopants of a same polarity as the source and drain regions, which is a significant deviation from using an operative MOSFET structure. Since there is no suggestion in the prior art relating to MOSFET-like antifuse devices of altering the

structure of the channel region such that it is substantially different from the structure of a conventional MOSFET, the present claims are considered novel and unobvious over the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

ERIK J. KIELIN
PRIMARY EXAMINER